Laboratory 4

(Due date: **002**: March 7th, **003**: March 8th, **004**: March 9th)

OBJECTIVES

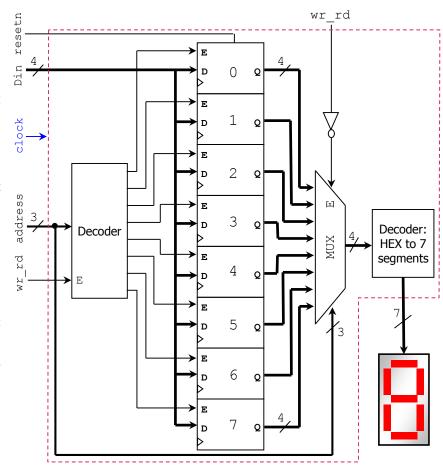
- ✓ Describe synchronous circuits in VHDL.
- ✓ Learn Testbench generation for synchronous circuits.

VHDL CODING

✓ Refer to the <u>Tutorial: VHDL for FPGAs</u> for a list of examples.

FIRST ACTIVITY (100/100)

- RANDOM MEMORY ACCESS (RAM)
 EMULATOR: The following circuit is a
 memory with 8 addresses, each address
 holding a 4-bit data. The memory
 positions are implemented by 4-bit
 registers. The resetn and clock
 signals are shared by all the registers.
 Data is written onto (or read from) one
 of the registers.
- Memory Write (wr_rd = 1): The 4-bit input Din is written into one register. The address[2..0] signal selects the register to be written. Here, the 7-segment display must show 0. Example: if address="101", then Din is written into register 5.
- Memory Read (wr_rd = 0): The MUX output appears on the 7-segment display (hex. value). The address[2..0] signal selects the register from which data is read. For example, if address= "010", then data in register 2 appears on the 7-segment display. If data in register 2 is "1010", then the symbol 'A' appears on the 7-segment display.



- ✓ Create a new ISE Project. Select the **XC7A100T-1CSG324 Artix-7 FPGA** device.
- ✓ Write the VHDL code for the given circuit. Create a separate file for i) Register with enable, ii) MUX with enable, iii) decoder with enable, iv) HEX-to-7 segments decoder, and v) top file.
- ✓ Write the VHDL testbench to test at least 8 writes onto memory and 8 reads from memory. You must generate a 100 MHz input clock for your simulations.
- ✓ Perform Functional Simulation and Timing Simulation of your design. **Demonstrate this to your TA**.
- ✓ I/O Assignment: Create the UCF file. Nexys-4 DDR: Use SW0 to SW7 for the inputs, CLK100MHZ for the input clock, CPU_RESETN push-button for resetn, and the 7-segment display for the output.
- ✓ Generate and download the bitstream on the FPGA and test. **Demonstrate this to your TA**.
- Submit (<u>as a .zip file</u>) all the generated files: VHDL code files, VHDL testbench, and UCF file to Moodle (an assignment will be created). DO NOT submit the whole ISE Project.

TA signature:	Date:
IA Signature.	Date.